Embedded ACPI Compliant DDR Power Generation Using the ISL6537 and ISL6506

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Introduction

The ISL6537, in conjunction with the ISL6506, provides a complete ACPI compliant power solution for computer systems with either dual channel DDRI or DDRII Memory systems. The chipset offered by Intersil provides the necessary control, protection and proper ACPI sequencing of the following rails: the 5V dual rail (5VDUAL), the 3.3V rail (3.3VDUAL), the DDR memory bias voltage (V_{DDQ_DDR}), the DDR memory termination voltage (V_{TT_DDR}), the DDR memory reference voltage (V_{REF_DDR}), the Graphic and Memory Controller Hub (GMCH) bias voltage (V_{GMCH}), and the GMCH and CPU termination voltage ($V_{TT\_GMCH/CPU}$).

The ISL6537 consists of a synchronous buck controller to supply V_{DDQ_DDR} with high current during S0/S1 (Run) states and standby current during S3 state (Suspend-To-RAM=STR). During Run mode, a fully integrated sink-source regulator generates an accurate and high current termination voltage. A buffered version of this voltage is provided as V_{REF_DDR}. The ISL6537 also features a dual stage LDO controller to regulate V_{GMCH} and a single stage LDO controller to regulate $V_{TT\_GMCH/CPU}$. A more complete description of the ISL6537 can be found in the datasheet[1].

The ISL6506 controls the 5VDUALs and 3.3VDUAL rails. There are three versions of the ISL6506. The version required will depend on whether 5VDUAL is to be active during S4/S5. A more complete description of the ISL6506 can be found in the datasheet[2].

Quick Start Evaluation

The ISL6537_6506EVAL1 board is shipped ‘ready to use’ right from the box. The ISL6537_6506EVAL1 supports testing with an ATX power supply. All seven outputs can be exercised through external loads. Both the V_{DDQ} and V_{TT} regulators have the ability to source or sink current while all other outputs may only source current.

There are posts available on each regulated output rail for attaching a load and/or monitoring the voltages. Eighteen individually labeled probe points are also available for use. These probe points provide Kelvin connections to signals which may be of interest to the user.

Two switches have been placed on the board to accommodate ACPI signal simulation. These two switches generate the SLP_S3 and SLP_S5 signals that are sent to the ISL6506, ISL6537 and turn off the ATX supply.

Recommended Test Equipment

To test the full functionality of the ISL6537 and ISL6506, the following equipment is recommended:

- An ATX power supply (minimum 160W configuration)
- Multiple electronic loads
- Four channel oscilloscope with probes
- Precision digital multimeters

As there are seven regulated rails, it is difficult to exercise and monitor all of them at the same time. The user may wish to employ discrete resistive loads in addition to electronic loads. Electronic loads are favored because they allow the user to apply a multitude of varying load levels and load transients which allow for a broader analysis.

Circuit Setup

SET SWITCHES

Ensure that the S3 switch is in the ACTIVE position and the S5 switch is in the S5 position. With the switches in these positions, the board will be forced into an S5 sleep state at initial power up.

CONNECT THE ATX SUPPLY

Plug the 20-pin connector from the ATX power supply into the 20 pin receptacle, J1, on the evaluation board. Should the ATX power supply have a master AC switch, turn this switch to the OFF position prior to applying AC voltage.

CONNECT LOADS

Figure 1 details the locations of the available power, ground, and signal connection points on the ISL6537_6506EVAL1 evaluation board The maximum loads specified for each rail below are absolute. All of the regulated rails are cascaded from the V_{DDQ_DDR} rail, which itself is cascaded from the 5VDUAL rail (refer to “ISL6537_6506EVAL1 Schematic” on page 9). Any loading of a cascaded rail will itself be a load on the rail that is providing input and must be accounted for prior to application of loads.

Loading V_{DDQ_DDR} - Sourcing Current: Connect the positive terminal of an electronic load to the VDDQ post. Connect the return terminal of the same load to the corresponding GND post. The maximum load current that the rail will support prior to entering an over-current condition is 15A.

Loading V_{DDQ_DDR} - Sinking Current: Typically, the V_{DDQ} rail does not sink current, however, the ISL6537 has the ability to allow the V_{DDQ} rail to do just that. To test the V_{DDQ} rail while sinking current, connect the positive terminal of an electronic load to the 5VDUAL post. Connect the return terminal of the same load to the VDDQ post. The maximum load current that the rail will support prior to entering an over-current condition is 15A.

CAUTION: The return terminal of the load must float for this to work properly.

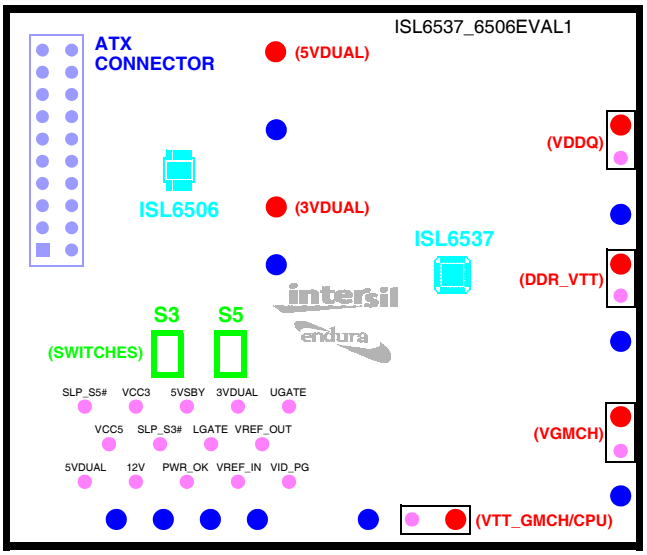


FIGURE 1. ISL6537_6506EVAL1 BOARD POWER AND SIGNAL CONNECTIONS

Loading V_{TT_DDR} - Sourcing Current: To test V_{TT_DDR} while the regulator sources current, connect the positive terminal of an electronic load to the DDR_ VTT post. Connect the return terminal of the same load to the corresponding GND post. The maximum continuous current that the rail will support is 2A. Transient loads to 3A are also supported.

Loading V_{TT_DDR} - Sinking Current: To test V_{TT_DDR} while the regulator sinks current, connect the positive terminal of an electronic load to the VDDQ post. Connect the return terminal of the same load to the DDR_VTT post. The maximum continuous current that the rail will support is 2A. Transient loads to 3A are also supported.

CAUTION: The return terminal of the load must float for this to work properly.

Loading V_{GMCH}: Connect the positive terminal of an electronic load to the VGMCH post. Connect the return terminal of the corresponding GND post. The maximum load supported by this rail is 10A.

Loading $V_{TT\_GMCH/CPU}$: Connect the positive terminal an electronic load to the VTT_GMCH/CPU post. Connect the return terminal of the corresponding GND post. The maximum load supported by this rail is 5A.

Loading 5VDUAL: Connect the positive terminal of an electronic load to the 5VDUAL post. Connect the return terminal of the corresponding GND post. The maximum load supported by this rail is 14A.

Loading 3VDUAL: Connect the positive terminal of an electronic load to the 3VDUAL post. Connect the return terminal of the corresponding GND post. The maximum load supported by this rail is 14A.

Operation

APPLY POWER TO THE BOARD

Plug the ATX supply into the mains. If the supply has an AC switch, turn it on. With the S3 and S5 switches in the ACTIVE and S5 positions, respectively, the board will be in the S5 sleep state. Voltages present on the board will be 5VSBY which is supplied by the ATX and 3VDUAL which is controlled by the ISL6506.

To enable the circuit, toggle the S5 switch to ACTIVE. This will place the board in the S0 state. All outputs should be brought up.

EXAMINE START-UP WAVEFORMS AND OUTPUT QUALITY UNDER VARYING LOADS

Start up is immediate following the transition to the S0 state. Using an oscilloscope or other laboratory equipment, the ramp-up and/or regulation of the outputs can be studied. Loading of the output can be accomplished through the use of an electronic load. Other methods, such as the use of discrete power resistors will work for loading as well.

Reference Design

General

The ISL6537_6506EVAL1 is an evaluation board that highlights the operation of the ISL6537 and ISL6506 in an embedded ACPI and DDR DRAM Memory Power application. The V_{DDQ_DDR} supply has been designed to supply 1.8V at a maximum load of 15A. The V_{TT_DDR} termination supply will track the V_{DDQ_DDR} supply at 50% while sourcing or sinking current. The dual stage LDO is designed to supply up to 10A of current at 1.5V for V_{GMCH} while the single stage LDO supplies 1.2V at up to 5A for $V_{TT\_GMCH/CPU}$. Refer to “ISL6537_6506EVAL1 Schematic” on page 9, “ISL6537_6506EVAL1 Bill of Material” on page 10 and “ISL6537_6506EVAL1 Layout” on page 11.

Power Up and State Transitions

There are several distinct state transitions that the ISL6537 and ISL6506 support. These include a Cold/Mechanical Start (S5 to S0 state transition), Active to Sleep (S0 to S3 transition), Sleep to Active (S3 to S0 transition) and finally Active to Shutdown (S0 to S5 transition). Table 1 shows the switch positions and the corresponding ACPI states.

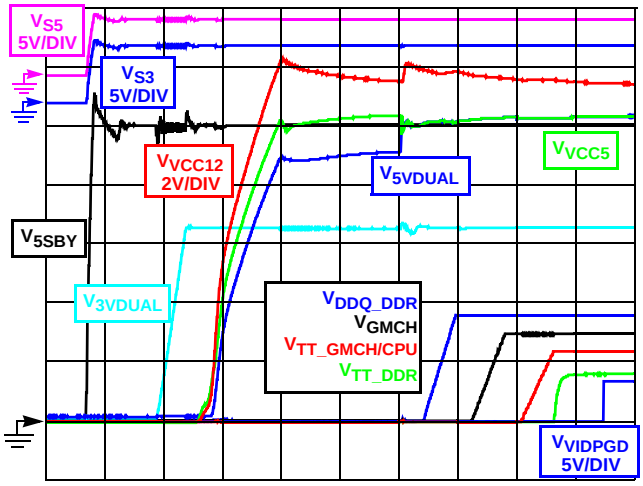
TABLE 1. ISL6537_6506EVAL1 STATES

S3 Switch	S5 Switch	SLEEP STATE	ATX STATE
ACTIVE	ACTIVE	S0 (Active)	ON
S3	ACTIVE	S3	Standby
ACTIVE	S5	S5	Standby
S3	S5	S5	Standby

If both the S3 and S5 switches are toggled simultaneously, the board will default to an S5 state. If the board is in either sleep state, the ATX supply is put into standby mode, where only the 5VSBY rail is active.

Initial Power Up - Cold Start

If both the S3 and S5 switches are toggled to the ACTIVE position prior to applying AC power to the ATX supply, the board will immediately enter into S0 state when the 5VSBY rail comes up after the AC power is applied to the ATX. Figure 2 shows a Cold Start-up sequence.

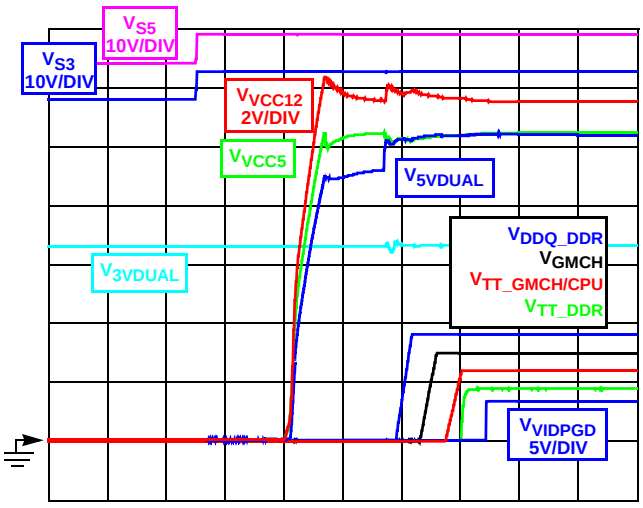


TIMEBASE: 10ms/DIV
ALL SIGNALS AT 1V/DIV UNLESS OTHERWISE STATED

FIGURE 2. COLD/MECHANICAL START

S5 Sleep State to S0 State Transition

If the S5 switch is toggled to the S5 position prior to application of AC power to the ATX supply, then the board will immediately enter into the S5 sleep state when the 5VSBY rail comes up after the AC voltage is applied to the ATX. The ISL6506 will bring up the 3VDUAL rail but all other output rails will be inactive. The transition from the S5 state to the S0 state will occur when the S5 switch is toggled to the ACTIVE position. Figure 3 shows this transition.



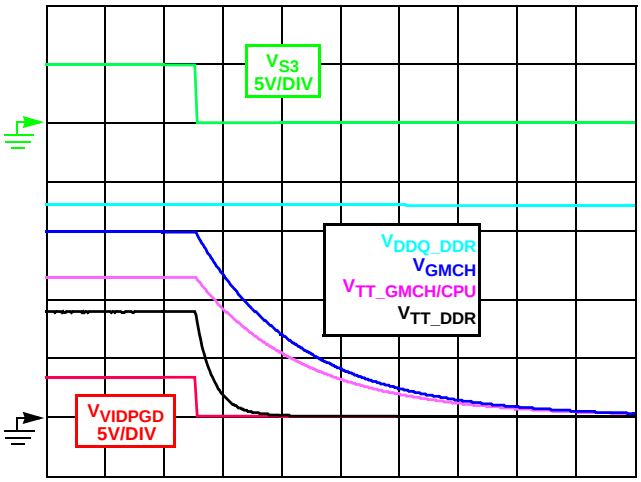
TIMEBASE: 20ms/DIV
ALL SIGNALS AT 1V/DIV UNLESS OTHERWISE STATED

FIGURE 3. S5 TO S0 STATE TRANSITION

Note that the 3VDUAL rail is already active prior to the other rails soft-starting. If the ISL6506A had been used, the 5VDUAL rail would have been active in the S5 state as well. Due to bulk capacitance, the voltage on the 5VDUAL rail may not experience a significant discharge if the board is placed into an S5 sleep state unless a load is applied.

S0 to S3 Sleep State Transition

Figure 4 shows the transition from the S0 state to the S3 sleep state. To achieve this transition, switch S3 is toggled to the S3 position. When transitioning from the S0 state to the S3 sleep state, it is important that the load on the V_{DDQ_DDR} rail be reduced to sleep state levels that the 5VDUAL rail is capable of supporting. If the load on V_{DDQ_DDR} is excessive, V_{DDQ_DDR} voltage will collapse.

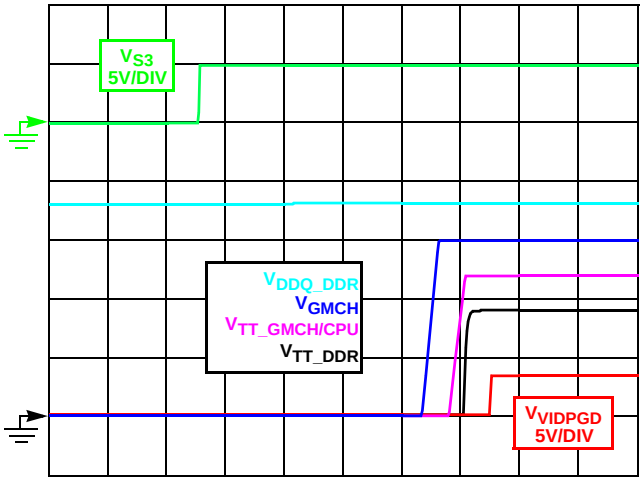


TIMEBASE: 100ms/DIV
ALL SIGNALS AT 500mV/DIV UNLESS OTHERWISE STATED

FIGURE 4. S0 TO S3 STATE TRANSITION

S3 to S0 State Transition

Figure 5 shows the transition from the S3 sleep state to the S0 state. This transition is accomplished by returning the S3 switch to the ACTIVE position. Once the PGOOD signal has been asserted, the V_{DDQ_DDR} rail can then be loaded beyond the S3 load limitations of 5VDUAL.



TIMEBASE: 20ms/DIV
ALL SIGNALS AT 500mV/DIV UNLESS OTHERWISE STATED

FIGURE 5. S3 TO S0 STATE TRANSITION

ACPI Start Up Timing

The ISL6506 and ISL6537 chipset were designed to work in tandem to start up critical voltages within a specific window during the overall start up or sleep recovery process of a typical motherboard. Figure 6 shows a generic desktop sleep state to wake state sequencing.

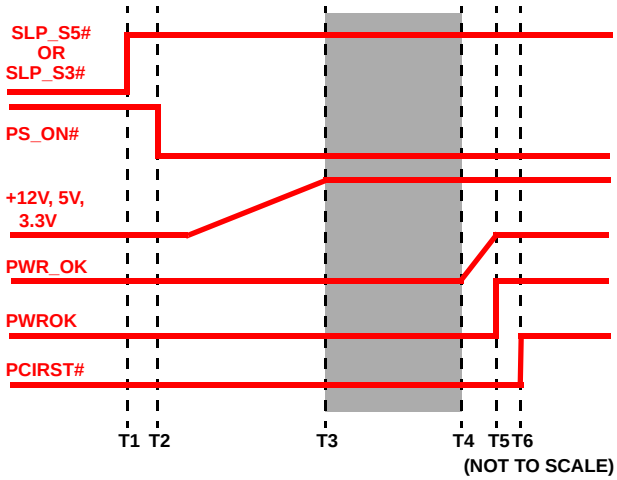


FIGURE 6. GENERIC WAKEUP SEQUENCING

At time T1, either the SLP_S3# or SLP_S5# signal transitions HIGH, which is the signal to the system to enter into the S0 state. At time T2, 10ns later, PS_ON#, the signal that commands the ATX supply to turn on, is forced LOW. At time T3, the ATX rails have risen to 95% of their targeted nominal levels. The time between T2 and T3 can be between 100ms and 500ms. At time T4, the PWR_OK signal from the ATX supply starts to rise. The time between T3 and T4 will also fall between 100ms and 500ms. At time T5, the ATX PWR_OK signal has risen HIGH. This transition is specified to be less than 10ms. At this point, the PWROK signal from the GMCH is commanded HIGH. At time T6, anywhere from 31 to 44 Real Time Clocks (RTCs) after PWROK has asserted HIGH, the PCIRST# signal from the Input/Output Controller Hub (ICH) asserts HIGH. When PCIRST# asserts HIGH, bus traffic resumes and the system is awake.

The ISL6506 and ISL6537 chipset bring all the ACPI rails under their control into regulation between time T3 and T4. This timing assures, even with minimum specified system timings, that the regulators will have their inputs available from the ATX supply and also that the output rails will be in regulation and ready for bus traffic once PCIRST# asserts HIGH.[4][5]

Evaluation Board Design

The complete Bill of Material for the evaluation board can be seen in “ISL6537_6506EVAL1 Bill of Material” on page 10. This section gives an overview of the design parameters and decisions made for each regulator.

ISL6506 Circuitry

The ISL6506 incorporates all the ACPI timing, control and monitoring required for the 5VDUAL and 3.3VDUAL rails, while maintaining a low component count. The Vishay Si7840 was utilized for both N-Channel MOSFET pass elements due to the low $R_{DS(ON)}$ and thermal capabilities of the packaging. Very little power is dissipated from the MOSFET in this application. The P-Channel MOSFET, the Vishay Si7483, was chosen for similar reasons.

The MOSFET thermal capabilities and it’s Rds(on) are the two major considerations when choosing a MOSFET as a pass element for the 5VDUAL and 3.3VDUAL rails. The maximum allowable temperature rise of the MOSFET is used to calculate the maximum power that the MOSFET can dissipate via the thermal resistance ratings of the FET. The maximum Rds(on) of the MOSFET can then be calculated by dividing the maximum allowable power dissipation of the MOSFET by the square of the maximum load current that will flow through the MOSFET. If the datasheet specified Rds(on) of the MOSFET being considered is less than this calculated maximum Rds(on) value, then the MOSFET can be used safely in the application, provided proper layout techniques for thermal dissipation are used.

ISL6537 Circuitry

V_{DDQ_DDR} SWITCHING REGULATOR

The V_{DDQ_DDR} switching regulator was designed to handle a 15A continuous output load while maintaining 1.8V. Voltage excursions due to transient loading of 25A/µsec were to be no greater than 50mV with a full 15A load step.

In order to supply 15A of continuous current with a duty cycle near 50%, two upper and two lower MOSFETs were utilized. The part chosen for both upper and lower MOSFETs was the Vishay Si7840BDP. The choice of both the MOSFET and the parallel MOSFET configuration will actually allow for a continuous current of at least 20A without the FETs becoming too hot.

The transient specifications were met by employing large value capacitors that have relatively low ESR ratings and by using some ceramic capacitors to decrease the effective ESR even more. Three 1800µF bulk capacitors with 16mΩ ESR were utilized as the bulk output capacitance. During a transient, the large capacitance supplies energy to the load while the output inductor current slews up to match the load current.

The output inductor was designed so that the ripple voltage on the output rail would be approximately 20mV. A simple wirewound toroidal inductor was designed for this regulator. To save on the Bill of Material (BoM) cost, the same inductor was used on the input filter to the V_{DDQ} regulator.

Since there is an input inductor, the input capacitors must be rated to handle all of the AC RMS current going through the upper MOSFET. The capacitors that were chosen have RMS current ratings that exceed the maximum RMS current expected at full load.

The final aspect to the V_{DDQ_DDR} regulator design was to insure the stability of the system. A Type III compensation network was chosen for this design. The compensation components were calculated to give a system bandwidth of about 50kHz with a Phase Margin of approximately 65°. For more information on calculating the compensation components for a single phase buck regulator, see Intersil's Technical Brief, TB417, titled "Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators."[3]

LDO REGULATORS

The V_{TT_DDR} regulator required minimal design work as the control circuitry and pass element are incorporated within the ISL6537. Except for the pass element and output capacitance, all other circuitry for the remaining LDOs is also contained within the ISL6537.

The V_{GMCH} LDO is a dual stage LDO. The dual stage LDO allows a larger load current to be applied to the output without dissipating excessive power through a single pass element. The ISL6537 was designed so that both linear stages will dissipate the same amount of power. With the 1.8V V_{DDQ_DDR} rail as the input to the V_{GMCH} LDO, the total drop is only 300mV with the output regulated at 1.5V. With a 10A load on V_{GMCH}, this results in 1.5W of dissipation through each MOSFET pass device. The Vishay Si7840BDP was chosen for both pass elements. The packaging of this device allows for efficient thermal dissipation to the board while supplying full load current.

The $V_{TT\_GMCH/CPU}$ LDO is a single stage LDO. Again, the pass element chosen was the Vishay Si7840BDP. This allowed for a higher single part count on the BoM while allowing this regulator to source a sufficient amount of load.

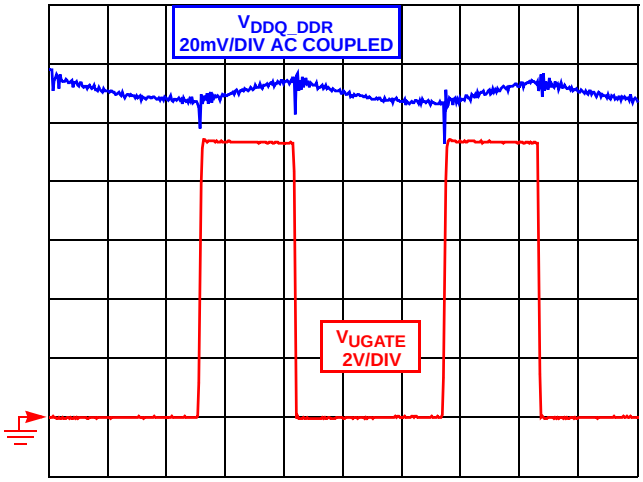
For all the LDOs, including the V_{TT_DDR} regulator, the output capacitance was chosen to maintain a stable output rail while minimizing voltage excursions due to load transients.

Evaluation Board Performance

This section presents the performance of the ISL6537_6506EVAL1 evaluation board while subjected to various conditions.

VDDQ_DDR Ripple Voltage

Figure 7 shows the ripple voltage on the V_{DDQ} output.

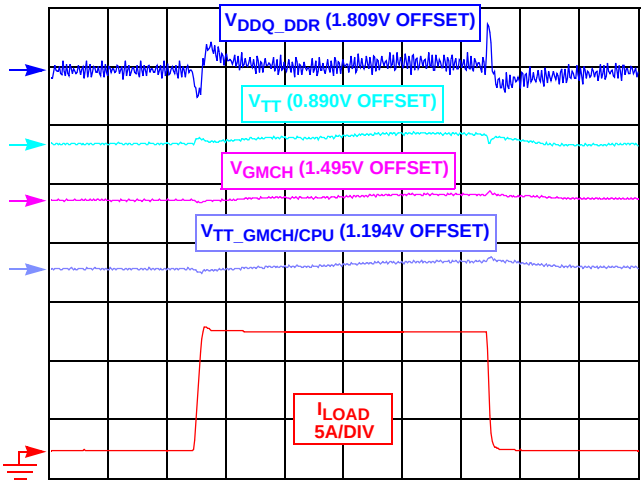


TIMEBASE: 1µs/DIV

FIGURE 7. V_{DDQ_DDR} RIPPLE VOLTAGE

Transient Performance

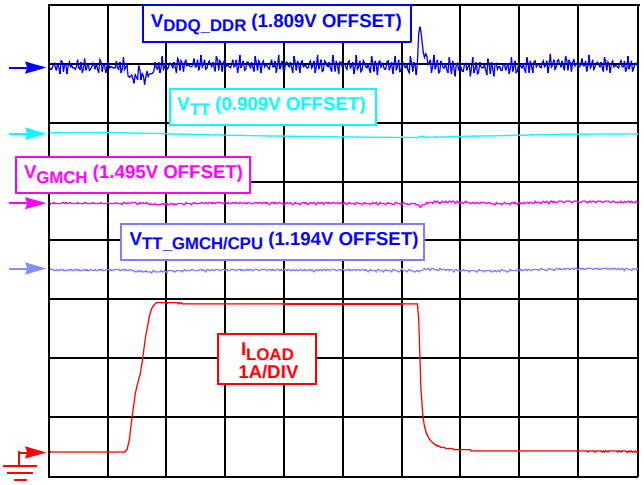
Figures 8 through 12 show the response of the outputs when subjected to a variety of transient loads while in the Active (S0) State. Figure 8 shows V_{DDQ_DDR} under transient loading. The response of the V_{DDQ_DDR} regulator to the transient load brings the output voltage back into regulation very quickly.



TIMEBASE: 200ms/DIV
ALL SIGNALS AT 50mV/DIV UNLESS OTHERWISE STATED

FIGURE 8. TRANSIENT ON V_{DDQ}

Figure 9 shows V_{TT_DDR} under a transient loading that causes V_{TT_DDR} to source current.

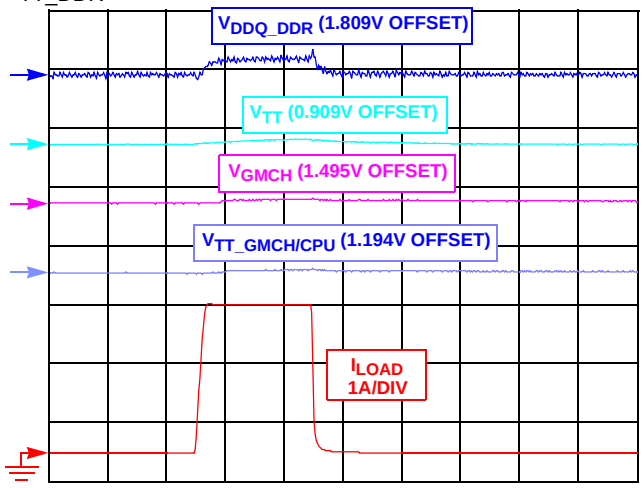


TIMEBASE: 200ms/DIV
ALL SIGNALS AT 50mV/DIV UNLESS OTHERWISE STATED

FIGURE 9. SOURCING TRANSIENT ON V_{TT_DDR}

While the load is being applied to the V_{TT_DDR} rail, there is a noticeable reaction in the V_{DDQ_DDR} rail as well. Since the V_{TT_DDR} rail is derived from the V_{DDQ_DDR} rail, any load on the V_{TT_DDR} rail is seen by the V_{DDQ_DDR} rail.

Figure 10 shows V_{TT_DDR} under a transient that causes V_{TT_DDR} to sink current.

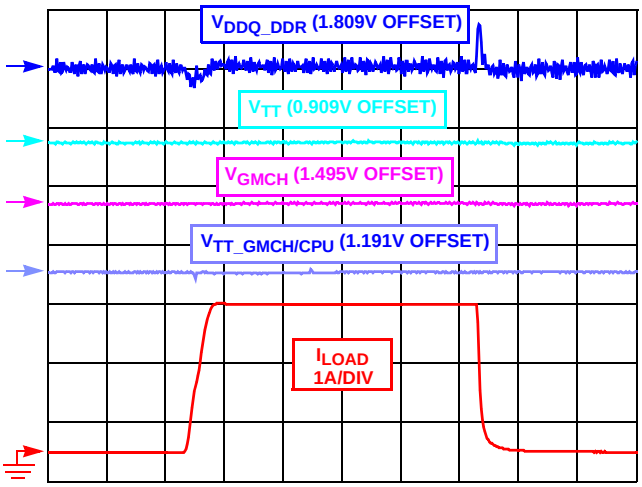


TIMEBASE: 500ms/DIV
ALL SIGNALS AT 50mV/DIV UNLESS OTHERWISE STATED

FIGURE 10. SINKING TRANSIENT ON V_{TT_DDR}

Again, the reaction of the V_{DDQ_DDR} rail is evident since the loading on the V_{TT_DDR} rail is transferred directly to the V_{DDQ_DDR} rail. In both cases, sourcing and sinking current, where the V_{TT_DDR} rail has been loaded and the V_{DDQ_DDR} rail has responded to the loading, the V_{TT_DDR} rail did not appear to be affected as much as the V_{DDQ_DDR} rail. This is because a linear regulator (V_{TT_DDR}) will respond much faster than a switching regulator (V_{DDQ_DDR}). This is because the inductor current must slew up/down to supply the load current while the linear regulator control will apply more voltage to the gate of the pass FET.

Figure 11 shows both V_{GMCH} under transient loading.

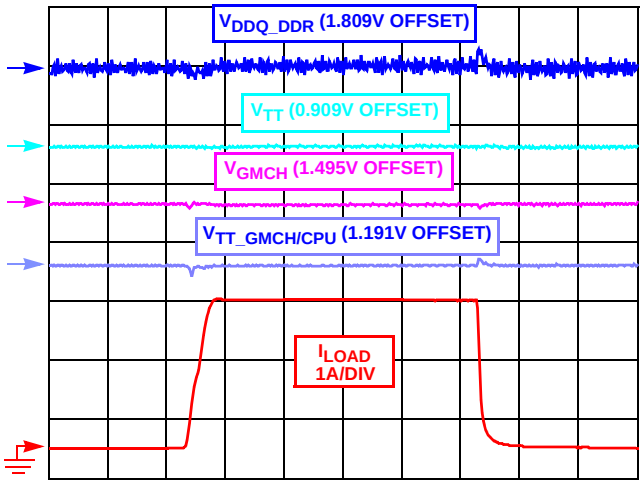


TIMEBASE: 500ms/DIV
ALL SIGNALS AT 50mV/DIV UNLESS OTHERWISE STATED

FIGURE 11. TRANSIENTS ON V_{GMCH}

Here, too, the linearly regulated V_{GMCH} rail is not affected as much as the V_{DDQ_DDR} rail which acts as the source rail for the V_{GMCH} regulator.

Finally, Figure 12 shows the $V_{TT\_GMCH/CPU}$ rail under transient loading.



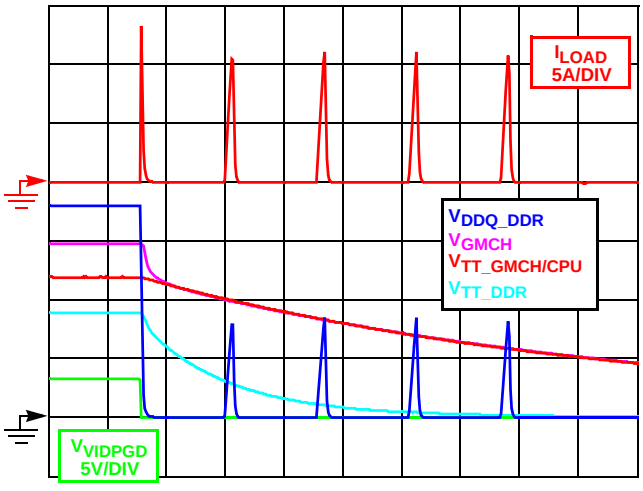
TIMEBASE: 200ms/DIV
ALL SIGNALS AT 50mV/DIV UNLESS OTHERWISE STATED

FIGURE 12. TRANSIENTS ON $V_{TT\_GMCH/CPU}$

The loading of this rail is light enough such that the response of the V_{DDQ_DDR} rail is negligible.

Fault Protection

Figure 13 shows response of the system to a fault on the V_{DDQ_DDR} rail.



TIMEBASE: 20ms/DIV
ALL SIGNALS AT 500mV/DIV UNLESS OTHERWISE STATED
100Ω LOAD ON V_{TT_DDR}, V_{GMCH}, and $V_{TT\_GMCH/CPU}$

FIGURE 13. FAULT RESPONSE

In this example of a fault, the VDDQ_DDR regulator output is shorted to ground. This causes an overcurrent fault response to occur. The VDDQ_DDR regulator is shut down and the internal fault counter increments from 0 to 1. As all the other regulators are cascaded from the VDDQ_DDR regulator, they are also disabled as well. The ISL6537 attempts to restart the system a total of four times with each attempt tripping an overcurrent fault and incrementing the fault counter by one. On the fourth failed retry, the internal fault counter reaches 5 and the system is shut down. The ISL6537 can only be restarted successfully by removing the cause of the fault and then either cycling the bias supply of the ISL6537 or putting the part into an S5 sleep state and then returning to the Run (S0) state.

Efficiency

Figure 14 shows the efficiency of the V_{DDQ_DDR} regulator while in the S0 State.

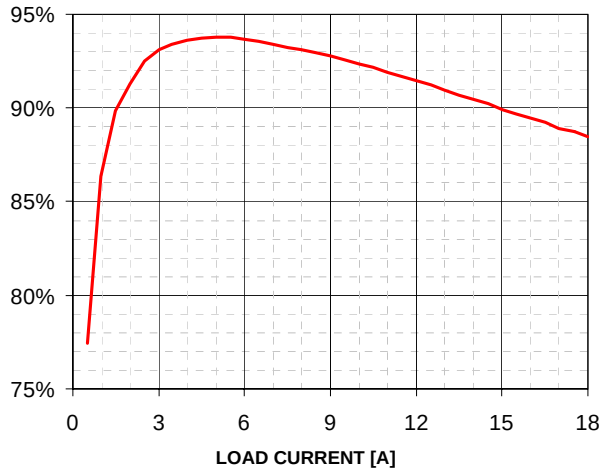


FIGURE 14. V_{DDQ_DDR} EFFICIENCY

Measurements were taken at room temperature under thermal equilibrium with no air flow. As the other regulated outputs are all derived through linear regulation, their efficiencies are not shown. The efficiency of the V_{DDQ_DDR} regulator is well above 90% for a majority of the loading range.

ISL6537_6506EVAL1 Customization

There are numerous ways in which a designer might modify the ISL6537_6506EVAL1 evaluation board for differing requirements. Some of the changes which are possible include:

- The input and output inductors, L200 and L201, for the V_{DDQ_DDR} regulator.
- The input and output capacitance for any of the regulators.
- The overcurrent trip point of the V_{DDQ_DDR} regulator, programmed through the OCSET resistor, R200. Refer to the ISL6537 datasheet for details on this.
- Changing the value of C104 to alter the soft start profile of the V_{TT_DDR} rail when transitioning from Sleep to Active State.
- All MOSFET footprints on the evaluation board allow for either SO8 or PowerPak packaged MOSFETs to be utilized.
- ISL6506 control can be bypassed by placing 0Ω jumpers at locations R15 and R18. Doing this will short out the NFETs that control the 3VDUAL and 5VDUAL rails.
- The output voltage of any regulator, except for V_{TT_DDR} may be modified by changing the voltage programming resistor for the respective regulator. For V_{DDQ_DDR}, change R204; for V_{GMCH}, change R302; for $V_{TT\_GMCH/CPU}$, change R401. If the voltage level is to be modified, always change the resistor that is tied between the feedback point of the error amplifier and ground. Modifying the value of the resistor that is located between the output and the feedback point on the error amplifier may alter the system response characteristics. Refer to the ISL6537 datasheet section titled “Output Voltage Selection” for the equations used to select the resistor values discussed above.
- The effect of the S3# and S5# signals on the ATX power supply can be negated by populating resistor Rx11 with a zero ohm jumper. Doing this will cause the PSON# signal to the ATX supply to be hard tied to ground. This will make the ATX supply stay on even in sleep states.

Conclusion

The ISL6537_6506EVAL1 is a versatile platform that allows designers to gain a full understanding of the functionality of the ISL6506 and ISL6537 chipset in an ACPI compliant system. The board is also flexible enough to allow the designer to modify the board for differing requirements. The following pages provide a schematic, bill of materials, and layout drawings to support implementation of this solution.

References

For Intersil documents available on the web, see http://www.intersil.com/

[1] *ISL6537 Data Sheet,* Intersil Corporation, FN9099.

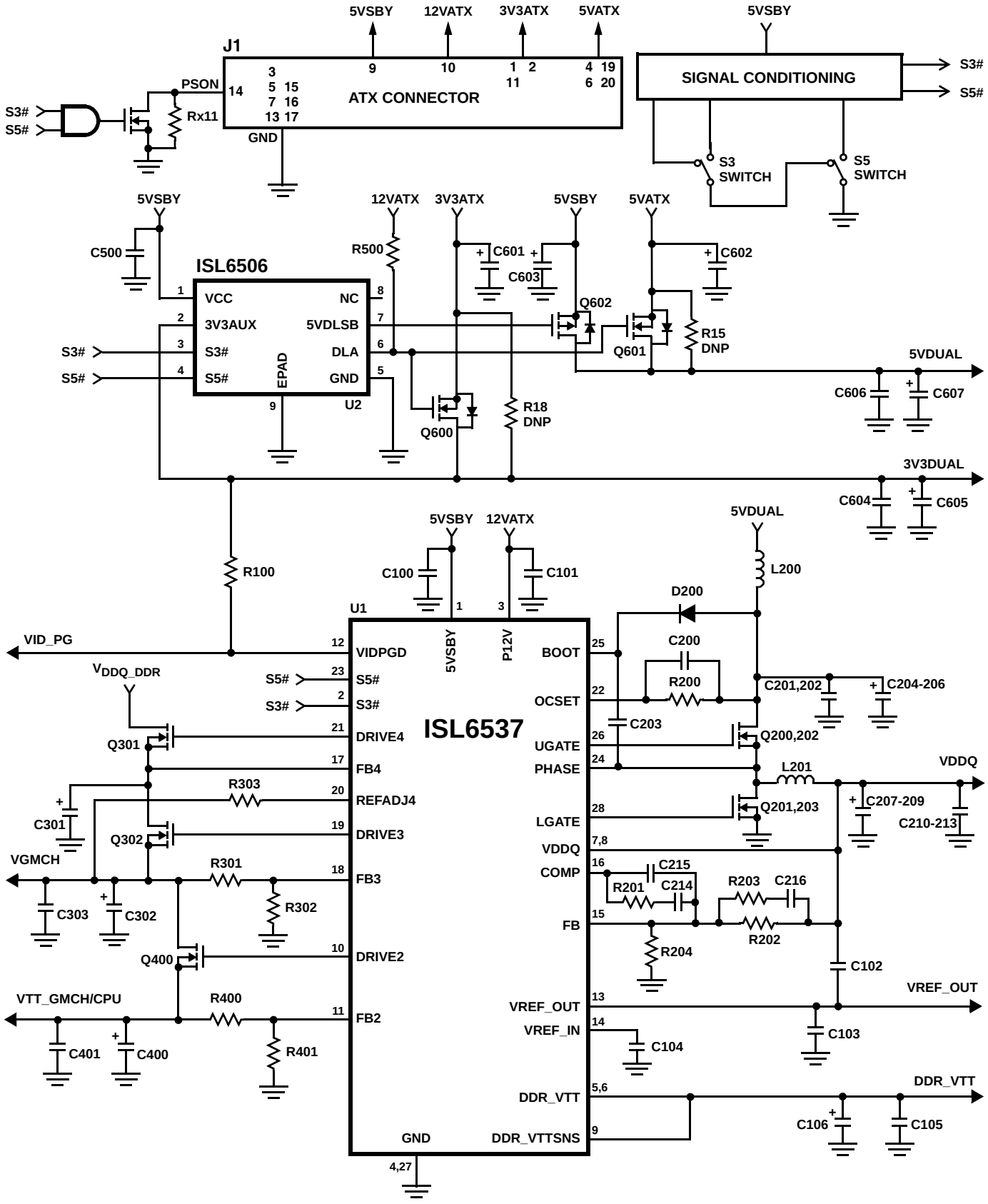
[2] *ISL6506 Data Sheet*, Intersil Corporation, FN9141.

[3] *Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators*, Intersil Corporation, TB417.

[4] *Advanced Configuration and Power Interface Specification, Revision 3.0a*, Hewlett Packard, Intel, Microsoft, Phoenix Technologies and Toshiba Corporations.

[5] *ATX Specification, Version 2.2*, Intel Corporation

ISL6537_6506EVAL1 Schematic



ISL6537_6506EVAL1 Bill of Material

REF DES	DESCRIPTION	PKG	VENDOR	VENDOR P/N	QTY
C100-103,203	0.1µF, 25V, X7R Ceramic Capacitor	0603	Various	-	5
C104	0.47µF, 10V, X5R Ceramic Capacitor	0603	Various	-	1
C105,210-213,302,401, 500,604,606	22µF, 6.3V, X5R Ceramic Capacitor	1206	Various	-	10
C106,301, 601-603	220µF, 25V, Al Electrolytic Capacitor	8x11.5	Panasonic	EEU-FCIE221	5
C200	1000pF, 100V, X7R Ceramic Capacitor	0603	Various	-	1
C204-206	2200µF, 6.3V, Al Electrolytic Capacitor	10x20	Rubycon	6.3MBC2200M10X20	3
C207-209, 303,400, 605,607	1800µF, 16V, Al Electrolytic Capacitor	10x23	Rubycon	16MBZ1800M10X23	7
C214	4700pF, 50V, X7R Capacitor	0603	Various	-	1
C215	1500pF, 50V, X7R Capacitor	0603	Various	-	1
C216	56nF, 25V, X7R Capacitor	0603	Various	-	1
D200	Diode	S-Mini	Panasonic	MA732	1
L200,201	2.2µH, 7T 14AWG on T50-52B Core	-	CoEv	MGPWL-00066	2
Q200-203, 301,302, 400,600	30V N-Channel MOSFET	PowerPak	Vishay	Si7840BDP	8
Q601	30V N-Channel MOSFET	PowerPak	Vishay	Si7880DP	1
Q602	30V P-Channel MOSFET	PowerPak	Vishay	Si7483DP	1
R100	10.0kΩ, 1% Resistor	0603	Various	-	1
R200	5.76kΩ, 1% Resistor	0603	Various	-	1
R201	31.6kΩ, 1% Resistor	0603	Various	-	1
R202,301	1.74kΩ, 1% Resistor	0603	Various	-	1
R203	21.0Ω, 1% Resistor	0603	Various	-	1
R204	1.37kΩ, 1% Resistor	0603	Various	-	1
R302	1.96kΩ, 1% Resistor	0603	Various	-	1
R303	0Ω Jumper	0603	Various	-	1
R400	1.24kΩ, 1% Resistor	0603	Various	-	1
R401	2.43kΩ, 1% Resistor	0603	Various	-	1
R500	1.00kΩ, 1% Resistor	0603	Various	-	1
U1	ACPI Compliant DDR Power Regulator	28ld 6x6mm QFN	Intersil	ISL6537CR	1
U2	ACPI Compliant Linear Power Regulator	8ld EPSOIC	Intersil	ISL6506CB	1

ISL6537_6506EVAL1 Layout

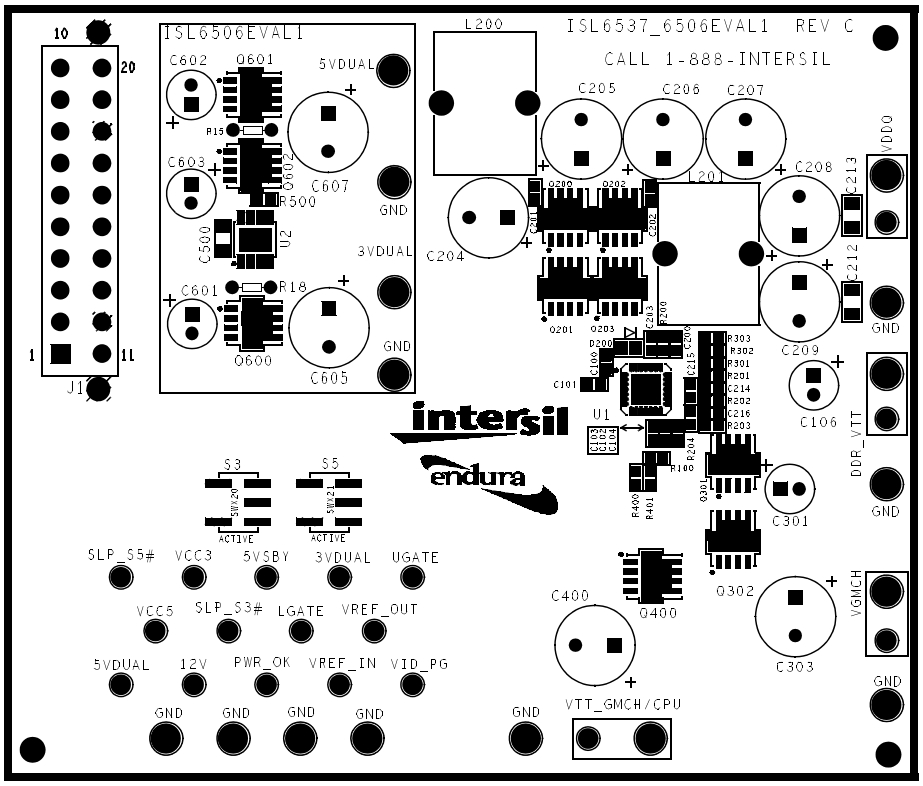


FIGURE 15. TOP SILK SCREEN

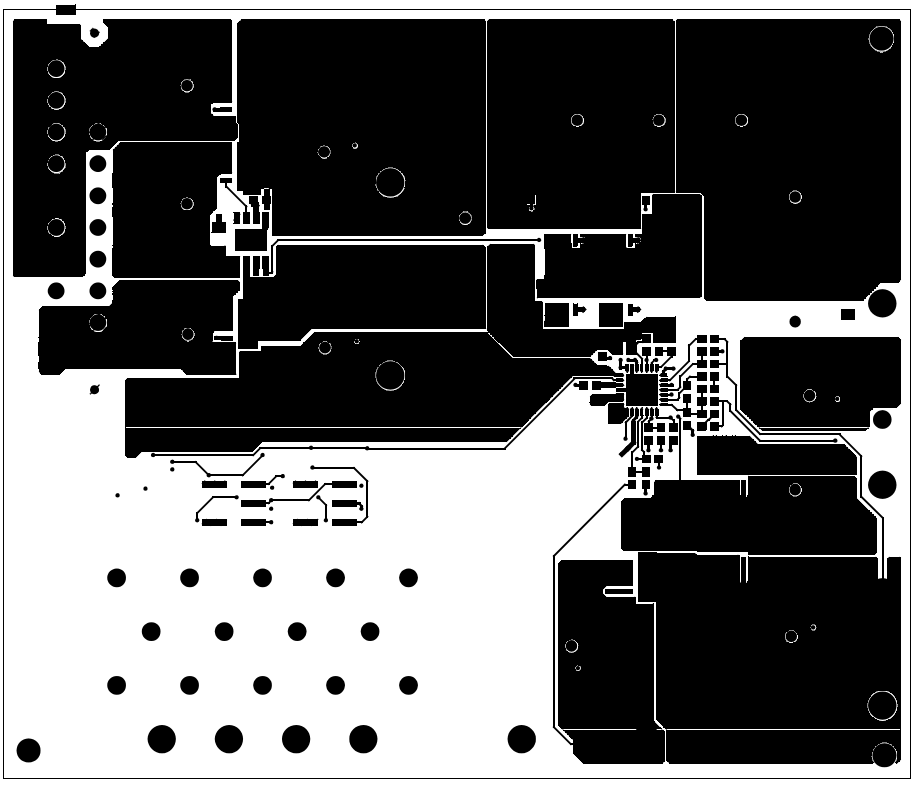


FIGURE 16. TOP

ISL6537_6506EVAL1 Layout (Continued)

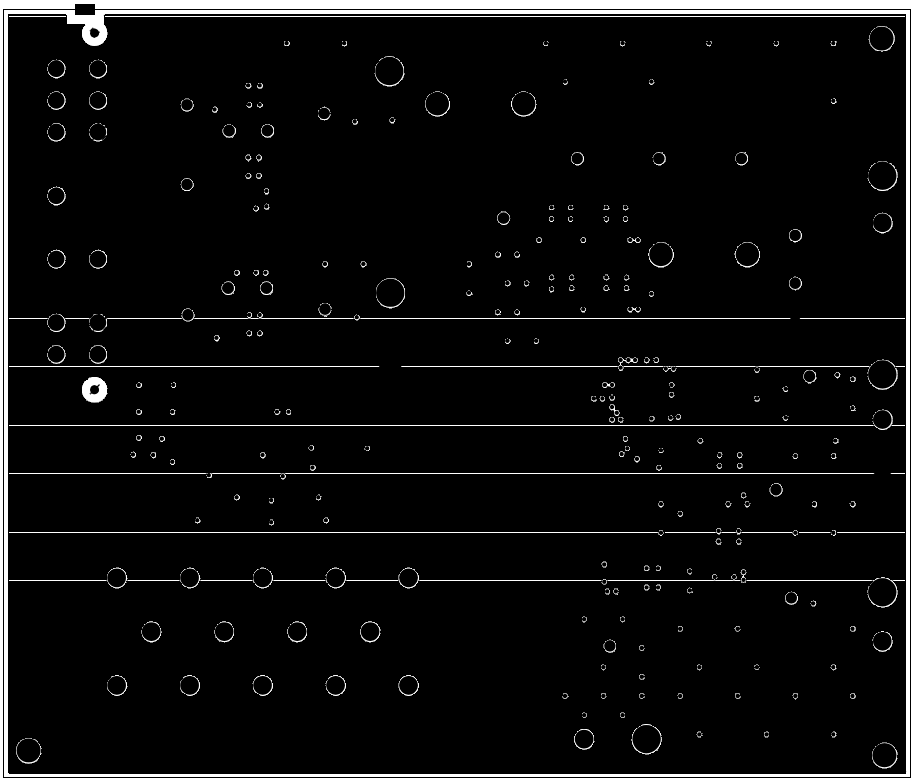


FIGURE 17. INTERNAL 1 GROUND

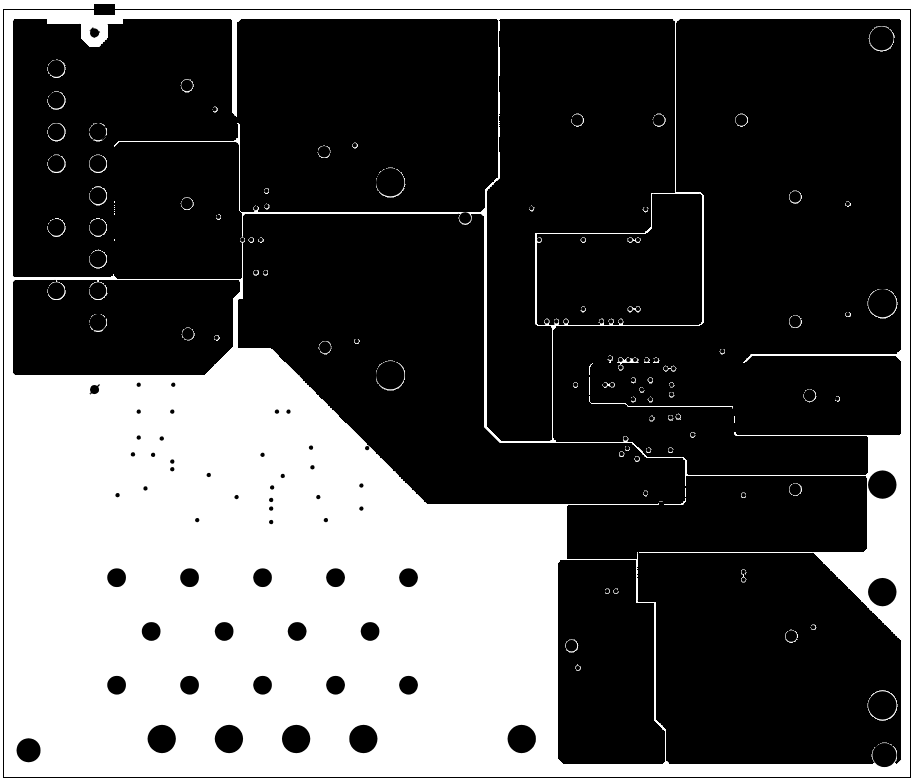


FIGURE 18. INTERNAL 2 POWER

ISL6537_6506EVAL1 Layout (Continued)

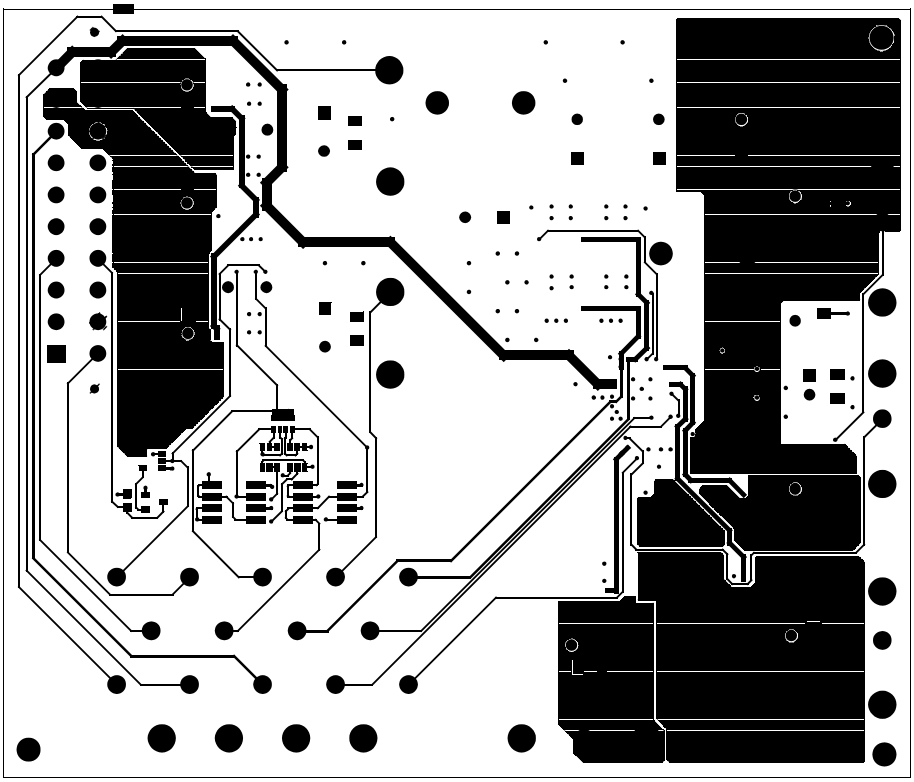


FIGURE 19. BOTTOM

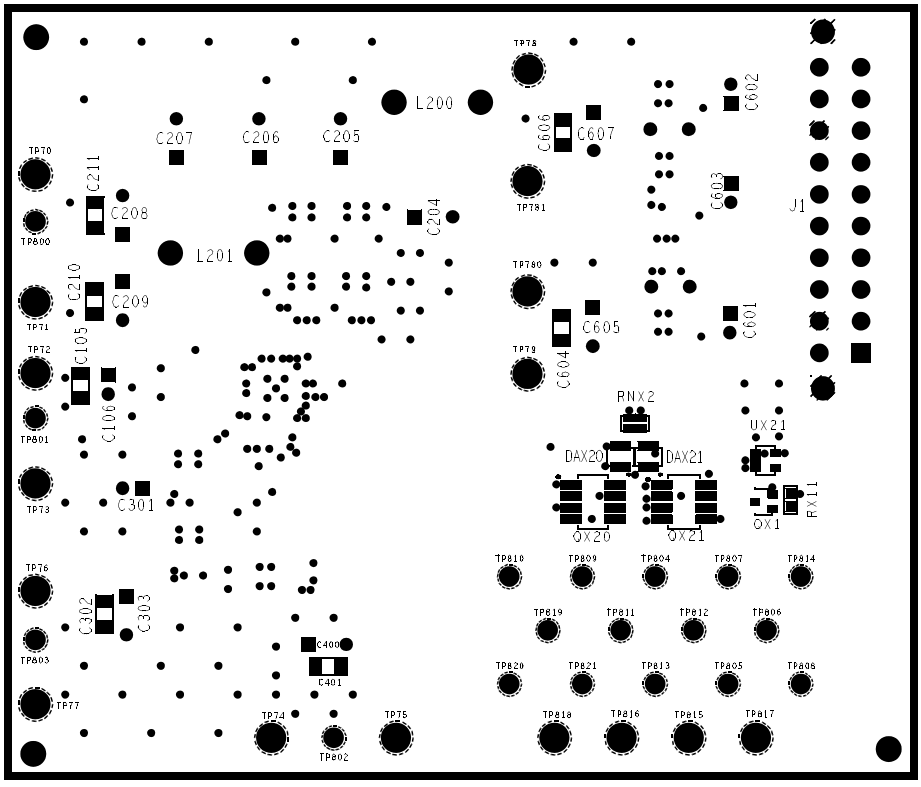


FIGURE 20. BOTTOM SILK SCREEN (*REVERSED*)